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# Development of a CMOS SOI Pixel Detector

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*Abstract*

We have developed a monolithic radiation pixel detector using silicon on insulator (SOI) with a commercial 0.15 $\mu$m fully-depleted-SOI technology and a Czochralski high resistivity silicon substrate in place of a handle wafer. The SOI TEG (Test Element Group) chips with a size of $2.5 \times 2.5$ mm$^2$ consisting of $20 \times 20$ $\mu$m$^2$ pixels have been designed and manufactured. Performance tests with a laser light illumination and a $\beta$ ray radioactive source indicate successful operation of the detector. We also briefly discuss the back gate effect as well as the simulation study.

## I. Introduction

A monolithic radiation pixel detector with the SOI technology is one of the position sensitive detectors that are able to overcome the difficulties in decreasing the pixel size and thickness, and the bump bonding employed by a hybrid pixel detector. The SOI pixel detector consists of a monolithic Silicon layer (handle wafer) covered with a insulating $SiO_2$ layer (Buried Oxide, BOX), and a thin Silicon film (device layer) over the BOX, in which a readout LSI is formed. The handle wafer is used for a radiation sensor with a matrix of depleted diodes directly connected to the LSI through a hole in the BOX. The SOI structure enables us to use two different types of silicon, i.e., the high resistivity silicon handle wafer for the radiation detection and the low resistivity silicon film for the readout electronics utilizing CMOS transistors.

Transistors formed on the SOI wafer can operate with higher speed and lower power consumption compared with the conventional bulk CMOS processes because of less parasitic capacitance [1]. Moreover, the SOI transistors are free from the latch-ups since individual transistors are completely separated by the BOX layer and have no PNPN parasitic structure. The thin device layer is insensitive to Single Event Upsets and Transients [2] due to its small energy deposit by ionizing radiations. Those SOI characteristics can satisfy the requirements of further improvement of the spatial resolution and radiation hardness imposed by future particle physics, astrophysics and medicine.

We have developed the SOI pixel detector in collaboration with OKI Electric Industry Co. Ltd. [3]. The basic technology of OKI's fully-depleted 0.15 $\mu$m CMOS SOI process [4] is employed. Additional processing steps for the implants to the handle wafer and contacts to it have also been developed. Figure 1 shows a cross-section of the SOI pixel detector.

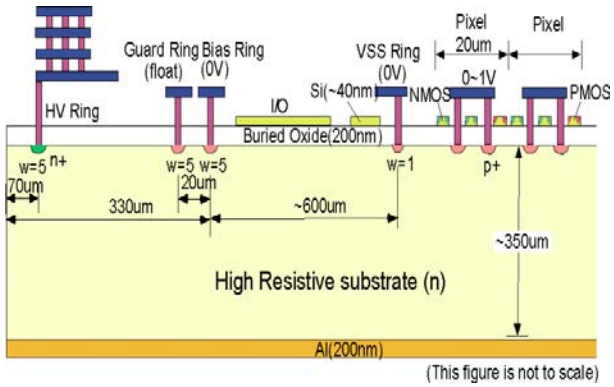


Figure 1: Cross-section of the SOI pixel detector.

## II. The SOI process

The SOI wafer is provided by SOITEC which employs the smart-cut procedure for the production. The wafer consists of a high resistive Cz silicon handle wafer ($>$ 1 k$\Omega$·m), a BOX layer with a thickness of 200 nm on the substrate and a p-type 50 nm thin Cz silicon film on the top in which transistors are formed. Since there is no original type assignment of the handle wafer and a possibility that the type could change during processing due to the thermal donor generation [5], we fabricated two kinds of TEG chips for p-type and n-type handle wafers.

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The implantation of p+ and n+ to the handle wafer and the formation of transistor drain and source implantation on the silicon film are performed simultaneously with the carrier density of about $10^{20}$ cm$^{-3}$ after opening holes in the BOX. This procedure can decrease the number of masks and process steps, and therefore costs. The implantation in the handle wafer is connected to a metal contact through the hole in the BOX. Three to five metal layers are formed on the silicon film for the circuit formation. Three different types of transistors are fabricated in the SOI process: high voltage transistors for I/O buffers, high threshold transistors utilized for normal logic and low threshold transistors used for high speed circuit. The pixel readout circuit employs the high threshold transistors with body ties.

The handle wafer having an original thickness of 650 $\mu$m is thinned to 350 $\mu$m, and its backside is plated with a 200 nm aluminum film. The detector bias can be applied from either the aluminum backside or pads on the top, both are connected to an n+ implant HV ring.

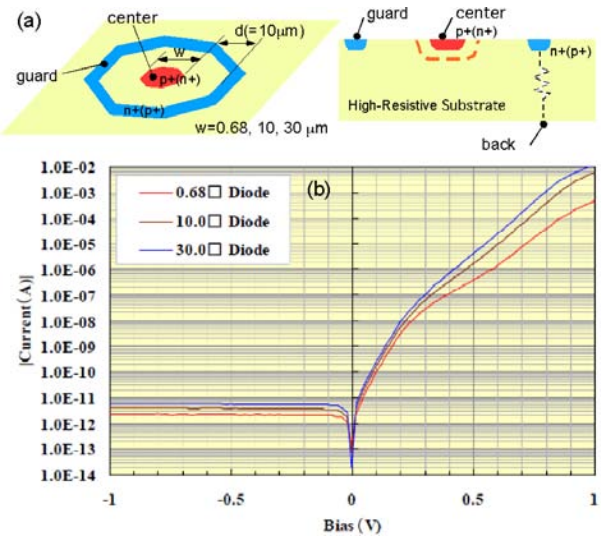


Figure 3: Measured I-V curve between p+ implant and the backside.

## III. Diode TEG

To determine the handle wafer type prior to process pixel TEG chip, we fabricated diode TEG chips having p+ and n+ implant in the handle wafer. Figure 2 shows a TEM picture of the cross section of the p+ implanted diode TEG and metal contacts to the first metal layer. The measured sheet resistance of p+ (n+) implant is 136 (33) Ω/squre. The $0.16 \times 0.16\ \mu$m$^2$ contact resistance is measured to be 218 (87) for p+ (n+) implant. We perform the I-V measurements for both p+ and n- implanted diode TEG. Figure 3 shows the curves of the diode TEG between p+ implant and the backside, indicating the diode characteristic and therefore the 'n' type handle wafer. We also measure the handle wafer resistivity with a four point probe to be 700 Ω·m, corresponding to the carrier density about $6 \times 10^{12}$ cm$^{-3}$.

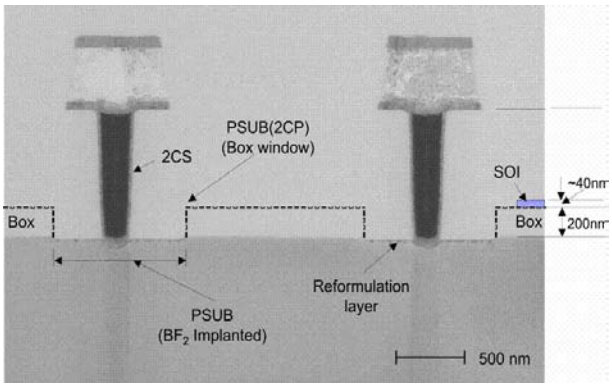


Figure 2: TEM picture of the cross section of the p+ implanted diode TEG and metal contacts to the first metal layer.

## IV. Pixel TEG

The $2.5 \times 2.5$ mm$^2$ pixel TEG chip consists of a $32 \times 32$ matrix of pixels with a size of $20 \times 20\ \mu$m$^2$. Figure 4 shows a picture of one pixel cell, which is composed of four $5.4 \times 5.4\ \mu$m$^2$ octagonal p+ implants and a storage capacitor of 100 fF. The pixel center is opened for a light illumination test. The accumulated charge is read out using correlated double sampling.

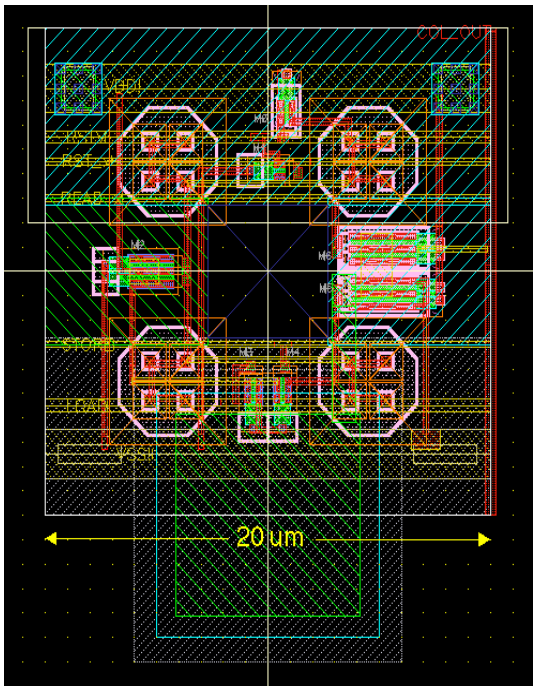


Figure 4: Picture of one pixel cell which is composed of four $5.4 \times 5.4\ \mu$m$^2$ octagonal p+ implants and a storage capacitor of 100 fF. The pixel center is opened for a light illumination test.

Figure 5 shows a I-V measured curve of the pixel TEG, where the bias voltage is applied from the backside Aluminum cover. The same curve is obtained by applying the bias to the HV ring pad. The breakdown happens when more than 98 V is applied, where the depletion thickness is about 140 $\mu$m. Using an infrared camera we find that the breakdown is caused by a hot spot around the corner of the bias ring. This can be cured by smoothing the corner and moving the ring inward. However, there is a much lower bias voltage limit for the proper operation of the pixel TEG readout due to the back gate effect described in the next section.

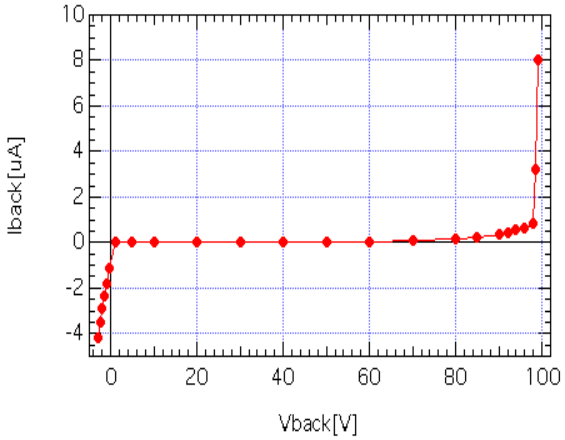


Figure 5: I-V measured curve of the pixel TEG.

We take a picture by illuminating red laser light (670 nm wavelength) with a plastic mask placed in front of the pixel TEG. We apply the detector bias of 10 V and expose it for 7 $\mu$s. Figure 6 shows an image obtained. From the size of the pixel window and the laser light intensity, we estimate the number of photons detected in the white part of the image to be $2 \times 10^4$; we expect 400 mV output signal height with 8 fF pixel capacitance. The measured signal amplitude is consistent with the expectation.

We also irradiate $\beta$ rays using a $^{90}$Sr source. Figure 7 shows an oscilloscope image of the pixel TEG output. The step in the picture indicates the $\beta$ ray signal. The size is measured to be 70 mV, which is consistent with the estimated collected charge of 0.6 fC (3500e) with the depletion thickness of 44 $\mu$m and the pixel capacitance of 8 fF.

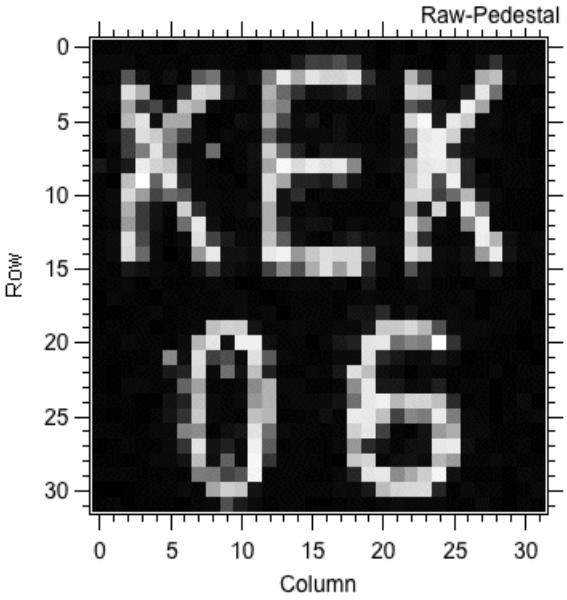


Figure 6: Picture taken using the pixel TEG with a red laser.

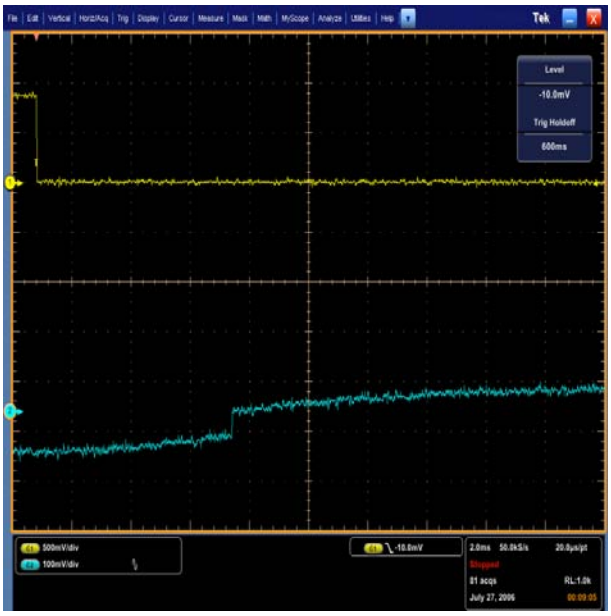


Figure 7: $\beta$ ray signal in the oscilloscope image of the pixel TEG output.

## V. Back Gate Effect

The transistors on the top Si film is affected by the potential level in the handle wafer, i.e. the transistor threshold voltage depends on the bias voltage applied to the handle wafer. Figure 8 shows measured threshold voltages of the three different types of transistors as a function of the bias voltage. The dependence is clearly seen, and the readout circuit is expected to stop its function with bias voltage more than 10 V. We confirm

this by observing the signal output of the I/O buffer. Figure 9 shows an oscilloscope image of the input and output signals of the I/O buffer. The output signal shape starts deviating when the bias voltage exceeds 15V. This behavior is also confirmed with a SPICE simulation.

Using a 3D TCAD simulation [6], we find that the back gate effect of an NMOS transistor can be reduced by implanting p+ in the handle wafer near the transistor position. We are optimizing the design and layout of the implant using the simulation.

## VI. Summary

We have started development of the SOI pixel detector using a commercial OKI 0.15 $\mu$m SOI process and SOITEC wafer. We identify the handle wafer type as 'n' and find that its resistivity is satisfactory for the radiation detection. The pixel TEG has been fabricated and tested. Photo images are successfully taken and $\beta$ ray signals are clearly detected. We find that the back gate effect can be removed by placing implantation near the transistors. The distance and shape of the implant is being optimized using the TCAD simulation.

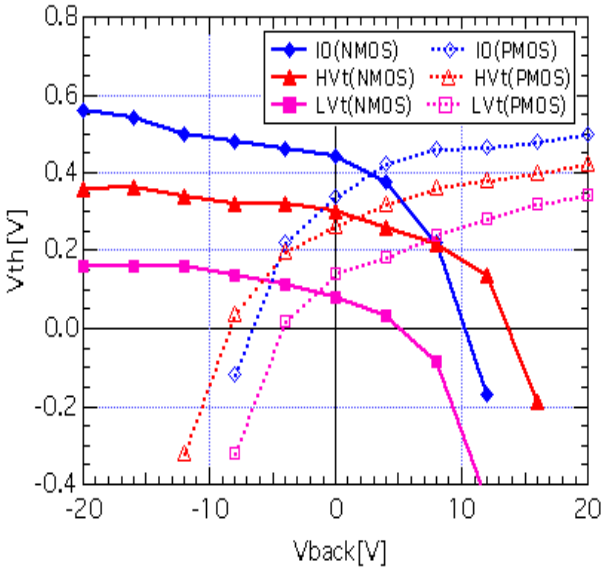


Figure 8: Measured threshold voltage (Vth) as a function of the bias voltage applied to the backside (Vback) for NMOS and PMOS transistors of three different types.

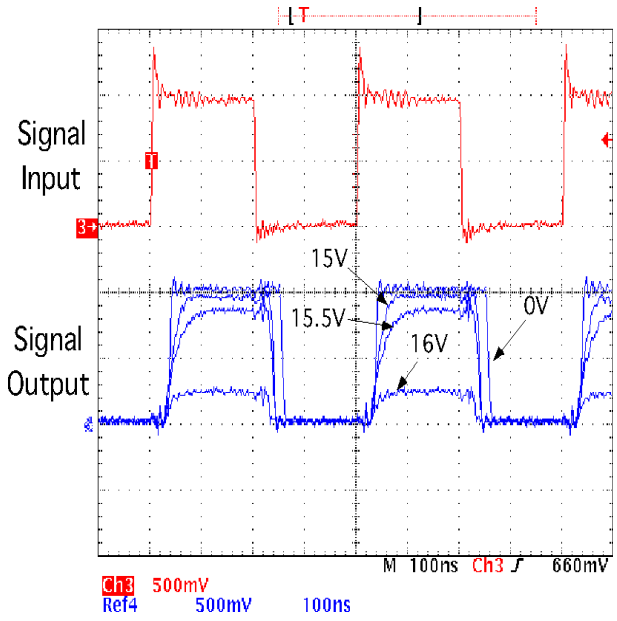


Figure 9: Oscilloscope image of the input and output signal of the I/O buffer. The output signal deviation becomes large as the bias voltage increases.

## References


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